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10/089,805	07/29/2002	Bin Yang	1516.1002/DMP	3090

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EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,805	YANG ET AL.	
	Examiner	Art Unit	
	Naheed Ejaz	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,18-22 and 23* is/are rejected.

7)☒ Claim(s) *11-17 and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/04/02 ,07/29/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: claim limitations are not properly deleted since it uses both close-ended brackets ']' (see page # 3, line 8 and line11) and makes it difficult to understand that which limitations applicant wants to delete since there is no open ended bracket in the claim. Appropriate correction is required.

(Note: all the limitations have been considered in this office action for claim 7).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Refer to claim 1, the preamble is claiming the method of correcting the digital frequency while it seems that body of the claim is correcting the phase (see claim 1). Clarification is required. Furthermore, claim 1 recites 'composing a predetermined (z (k)) of N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to arctan (2^{-n}), n= 0, 1, ..., N-1, and are respectively provided with sign (σ_n) providing a direction of rotation' (page # 2, lines 7-9), it is not clear that composing of angle and direction of rotation is in response to what part of the invention? Clarification is required.

4. As per claim 3, it recites the limitations of 's= 0, 1' (see page # 2, line 20) where 's' is not part of any of the parameters claimed and it is not stated what 's' is referring to. Appropriate correction is required.

5. Referring claim 18, it recites the limitations of 's= 0, 1' (see page # 4, line 24) where 's' is not part of any of the parameters claimed and it is not stated what 's' is referring to. Appropriate correction is required.

6. Claims 2, 4-6 and 19-21 are also rejected under 35 U.S.C. 112 second paragraph since they are based on rejected claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, in view of Jack E. Volder ('The Cordic Trigonometric Computing Technique,' *IRE Transactions on Electronic Computer,* Vol. EC-8, pp.330-334, September 1959), hereinafter referred to as Volder.

9. Refer to claim 1, Schroeder teaches, 'sampling a signal with a sampling cycle (k) and digitalized (x (k))' (see figure 3, element 302, figure 4, element 400, col.8, lines 4-20 & col.25, lines 55-66), 'processing an N-step CORDIC algorithm so that a frequency of a signal (x (k)) is altered at a predetermined frequency' (see figure 13, element 1312, col.25, lines 66-68, col.26, lines 1-58),'representing the signal (x (k)) a first vector comprising a first in-phase component (i_0) and a first quadrature component (q_0) in a

complex I/Q plane' (see figure 13, element 1308, col.26, lines 3-12) (it is noted that the real and imaginary components with respect to each sample (claimed x(k)) are considered to be a first vector of the claim since this vector is defined in complex plane with it's real and imaginary parts (claimed in-phase and quadrature components)), 'imaging the first vector by applying the CORDIC algorithm onto a second vector with a second in-phase component (I_n) and a second quadrature component (Q_N), wherein the second vector represents a signal with an altered frequency and phase' (see figure 13, elements 1312, 1313, 1316, & 1318, col.26, lines 16-41) (it should be noted that elements 1313 and 1318 (figure 13) are the vectors resulting from the cordic algorithm (figure 13, element 1312) with respect to the first vector of real and imaginary components (figure 13, element 1308) and hence is considered to be equivalent to applicant's limitations of imaging the first vector by applying cordic algorithm onto a second vector.

Schroeder does not explicitly disclose different rotation angles.

Volder discloses, 'composing a predetermined angle (z (k)) of N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to arctan (2^{-n}), n=0, 1,...,N-1, and are respectively provided with a sign (σ_n) providing a direction of rotation' (see figure 1, page # 331, col.1 & col.2, lines 1-18).

It would have been obvious to one ordinary skill in the art to implement the teachings of Volder into Schroeder in order to employ unique technique for solving the trigonometric relationships involved in plane coordinate rotation as taught by Volder

(see page # 334, col.2, 'conclusion') and thus recovered phase modulation information by analysis of the positions of the vectors in the complex planes.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, in view of Corleto et al. (US 6,192,089), hereinafter referred to as Corleto.

Refer to claim 7, Schroeder teaches, 'a delay element (see figure 8, elements 814-816 & 'Address delay'); and an adder adding a predetermined frequency value (f=T/m) to an output value of the delay element, outputting a result indicative thereof '(see figure 8, element 820, col.21, lines 9-14) (it is noted that 'control sequence (figure 8, element 820) is based on FIFO and an adder and as a result of it's function is adding the input values including their frequencies (claimed predetermined frequency) to the output of the delay elements (figure 8, elements 814-816) in order to perform the delay equalization function (see col.19, lines 45-68, col.20, 1-14 & lines 50-68) and hence is equivalent to applicant's limitations),'storing the result in the register, wherein the register value of a preceding cycle (k-1) is supplied to the delay element.' (see figure 8, elements 819 & 818, col. 19, lines 45-68, col.20, lines 1-14, col.25, lines 31-38) (it is noted that the mentioned elements are responsible to store the values and when is added to the whole process including delay and adder as described above becomes equivalent to the applicant's limitations in the claim).

Although Schroeder discloses a sign and cosine table (see figure 8, elements 801a & 801b, col.19, lines 45-68, col.20, lines 1-14) but he does not explicitly teach N micro-rotation blocks.

Corleto discloses, 'N micro-rotation blocks receiving a signal (i_0, q_0) (see figure 14, elements 142 & 148, col.6, lines 55-67, col.7, lines 1-36, col.9, lines 44-49) (it is noted that the mentioned elements are responsible to calculate the cordic algorithm steps including the calculation of arctan for in-phase and quadrature components in complex plane therefore is considered to be equivalent to applicant's limitations in the claim), 'a sign table providing to each micro-rotation block a sign (σ_n) from a sign table' (see figure 17 & 18, col.10, lines 59-67, col. 11, lines 1-42), 'a register driving the sign table and supplying a register value (w(k))' (figure 5, figure 16, element 192).

It would have been obvious to one ordinary skill in the art to implement the teachings of Corleto into Schroeder in order to prevent the communication system from having an error in a receiver frequency with respect to carrier frequency by filtering out the undesirable signal by applying the CORDIC vector rotation processor as taught by Corleto (see col.1, lines 49-58, col.4, lines 39-43, col.5, lines 15-26).

11. Claim 7 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, in view of Bruekers et al. (5,784,414), hereinafter referred to as Bruekers.

12. Refer to claim 7, Schroeder teaches, 'a delay element (see figure 8, elements 814-816 & 'Address delay'); and an adder adding a predetermined frequency value (f=T/m) to an output value of the delay element, outputting a result indicative thereof '(see figure 8, element 820, col.21, lines 9-14) (it is noted that 'control sequence (figure

8, element 820) is based on FIFO and an adder and as a result of it's function is adding the input values including their frequencies (claimed predetermined frequency) to the output of the delay elements (figure 8, elements 814-816) in order to perform the delay equalization function (see col.19, lines 45-68, col.20, 1-14 & lines 50-68) and hence is equivalent to applicant's limitations),'storing the result in the register, wherein the register value of a preceding cycle (k-1) is supplied to the delay element.' (see figure 8, elements 819 & 818, col. 19, lines 45-68, col.20, lines 1-14, col.25, lines 31-38) (it is noted that the mentioned elements are responsible to store the values and when is added to the whole process including delay and adder as described above becomes equivalent to the applicant's limitations in the claim),'a register driving the sign table and supplying a register value (w (k))'(see figure 6, element 625 or figure 8, elements 821-824).

Although Schroeder discloses a sign and cosine table (see figure 8, elements 801a & 801b, col.19, lines 45-68, col.20, lines 1-14) but he does not explicitly teach N micro-rotation blocks.

Bruekers discloses, 'N micro-rotation blocks receiving a signal (i_0, q_0) (see figure 1, elements 9 & 12, col.1, lines 15-39 or figure 12, elements 9 & 12) (it is noted that the mentioned elements are responsible to calculate the cordic algorithm steps including the calculation of arctan for in-phase and quadrature components in complex plane therefore is considered to be equivalent to applicant's limitations in the claim).

It would have been obvious to one ordinary skill in the art to implement the teachings of Bruekers into Schroeder in order to reduce the power consumption by

coupling more than one digital quadrature processors (claimed micro-rotation blocks) as taught by Bruekers (see col.2, lines 49-55).

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, and Corleto et al. (US 6,192,089, hereinafter referred to as Corleto, as applied to claim 7 above, and further in view of Bruekers et al. (5,784,414), hereinafter referred to as Bruekers.

Referring to claim 8, in addition to aforementioned rejection of claim 7, Schroeder and Corleto teach all the limitations in the previous claims on which claim 8 depends but they fail to disclose rotation of signal in first or fourth quadrant explicitly.

Bruekers discloses, 'rotating the signal into a first or fourth quadrant of the complex plane I/Q plane and providing a vector (i_0, q_0) representing the signal being rotated' (see figure 10a-10c, col.7, lines 8-19).

It would have been obvious to one ordinary skill in the art to implement the teachings of Bruekers into Schroeder and Corleto in order to reduce the power consumption by coupling more than one digital quadrature processors (claimed micro-rotation blocks) as taught by Bruekers (see col.2, lines 49-55).

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, and Corleto et al. (US 6,192,089, hereinafter referred to as Corleto, as applied to claim 7 above, and further in view of Collier et al. (5,052,050), hereinafter referred to as Collier.

Referring to claim 8, in addition to aforementioned rejection of claim 7, Schroeder and Corleto teach all the limitations in the previous claims on which claim 8 depends but they fail to disclose rotation of signal in first or fourth quadrant explicitly.

Collier discloses, 'rotating the signal into a first or fourth quadrant of the complex plane I/Q plane and providing a vector (i_0, q_0) representing the signal being rotated' (see figure 4 and 5, col.5, lines 15-25).

It would have been obvious to implement the teachings of the Collier into Schroeder and Corleto in order for demodulator to recover the modulation information correctly by removing the dc component of the I and Q signals because these signals represent the phase of the signal which would be used in detecting the frequency and thus enhance the system reliability as taught by Collier (see col.1, lines 45-58).

14. Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter referred to as Schroeder, Corleto et al. (US 6,192,089, hereinafter referred to as Corleto, Bruekers et al. (5,784,414), hereinafter referred to as Bruekers, as applied to claim 7 & 8 above, and further in view of Jack E. Volder ('The Cordic Trigonometric Computing Technique,' *IRE Transactions on Electronic Computer,* Vol. EC-8, pp.330-334, September 1959), hereinafter referred to as Volder.

Refer to claim 9, Schroeder, Corleto and Bruekers teach all the limitations in the previous claims but they do not show shift register of the micro-rotation block and accumulators adding the output values of the shift register explicitly.

Volder discloses, 'two shift registers shifting components of an input vector (I_n, Q_n) of the micro-rotation block by n bits and providing output values' (see figure 2, elements 'X Register' & 'Y Register'), 'two accumulators adding the components of the input vector (I_n, Q_n) to the output values of the shift registers, the output values of the shift registers being provided with the sign (σ_n) allocated to the respective micro-rotation block (see figure 2, elements 'Adder- Subtractor' & figure 3).

It would have been obvious to one ordinary skill in the art to implement the teachings of Volder into Schroeder, Corleto and Bruekers in order to employ unique technique for solving the trigonometric relationships involved in plane coordinate rotation as taught by Volder (see page # 334, col.2, 'conclusion') and thus recovered phase modulation information by analysis of the positions of the vectors in the complex planes.

15. Claim 22 is rejected under the same rational as mentioned in claim 9 rejection above.

16. Claims 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroeder et al. (4,884,265), hereinafter, referred to as Schroeder, Corleto et al. (US 6,192,089, hereinafter referred to as Corleto, Bruekers et al. (5,784,414), hereinafter referred to as Bruekers, Jack E. Volder ('The Cordic Trigonometric Computing Technique,' *IRE Transactions on Electronic Computer,* Vol. EC-8, pp.330-334, September 1959), hereinafter referred to as Volder, as applied to claims 7-9 above, and further in view of Welles, II et al.(4,603,300), hereinafter referred to as Welles.

Refer to claim 10, Schroeder, Corleto, Bruekers, and Volder teach all the limitations in the previous claims on which claim 10 depends as Shroeder and Corleto disclose sign table and micro-rotation blocks (see claim 7 rejection of this office action) but they fail to disclose XOR gates.

However, Welles teaches, 'a read-only memory comprising 2 (N-2) bits' (see col.7, lines 19-30), 'an XOR gate' (see figure 5, 8, or 9, col.6, lines 59-68, col.9, lines 31-54), 'an inverter' (see figure 7, element 76).

It would have been obvious to one ordinary skill in the art to implement the teachings of the Welles into Schroeder, Corleto, Bruekers, and Volder in order to recover the modulating signal including frequency components by obtaining the difference in successive binary numbers, a sequence of binary numbers representing successive levels of the modulating signal is obtained as taught by Welles (see col.3, lines 33-53, col.4, lines 38-55).

17. Claim 23 is rejected under the same rational as mentioned in claim 10 rejection above.

Allowable Subject Matter

18. Claims 11-17 and 24-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Claims 2, 4-6, and 19-21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Contact Information

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naheed Ejaz
Examiner
Art Unit 2631

N.E.
12/2/2005